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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,105	10/10/2001	Craig Nemecek	CYPR-CD00184	8788

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EXAMINER	
BRODA, SAMUEL	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,105	NEMECEK, CRAIG	
	Examiner	Art Unit	
	Samuel Broda	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-11* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/15/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 12-26, subject to the restriction requirement described below, have been examined.

Election/Restriction

2. As the claims are presented, restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-11, drawn to a method of programming a field programmable gate array (FPGA) by sending configuration data over the data lines so that the FPGA incorporates a specified interface, classified in class 703, subclass 28.

II. Claims 12-26, drawn to a method of communicating with a field programmable gate array (FPGA) by communicating over a communication interface, classified in class 703, subclass 23.

2.1 Inventions I-II are related as subcombination and combination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)).

In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination does not require a particular communication interface structure.

The subcombination of Group I has separate utility such as the automatic placement of an interface onto a FPGA during the manufacture of a particular circuit.

2.2 Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification and/or recognized divergent subject matter, restriction for examination purposes as indicated is proper.

2.3 On 11 April 2005, the Examiner telephoned Applicant's attorney Mr. Anthony Murabito, Reg. No. 35,295, regarding an election/restriction requirement. Mr. Murabito agreed to elect claims 12-26 without traverse. Applicant is requested to formally cancel claims 1-11 as part of any response to this Office action.

Priority

3. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is denied, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the

Application. In particular, no part of the provisional application appears to disclose the method steps shown in the Application at Fig. 7.

Drawings

4. Applicant's formal drawings have been reviewed and approved.

Claim Rejections - 35 U.S.C. § 112, Second Paragraph

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5.1 Claims 12-26 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are the method steps used to communicate over the communication interface and structural design of the communication interface.

As currently written, the preamble of each independent claim is directed to "a method of communicating with a field programmable gate array" and this function appears to be accomplished by a limitation that states in part: "communicating over a communication interface." This set of method steps appears circular.

Although are claims are written in method format, features of the structural design of communication interface are necessary to accomplish the claimed methods. Some of this information appears in the Specification in the "summar[y] [of] the significant connections of this interface" in Table 2 at page 25 lines 11-18.

Claim Rejections - 35 U.S.C. § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> . . .
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6.1 Claims 12-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim, U.S. Patent Application Publication US 2002/0116168 A1, published 22 August 2002 and filed 15 November 1999.

6.2 Regarding claim 12, Kim teaches a method of communicating with a field programmable gate array (FPGA), comprising:

communicating over a communication interface to configure the FPGA to function according to a programmed configuration [software download to the control FPGA 4 (page 2 paragraph 0035)]; and

carrying out communications over the communication interface to the FPGA functioning according to the programmed configuration [configuration of control FPGA 4 to set up an enhance parallel port or extended capabilities port in order to permit emulation system to communicate (page 2 paragraphs 0036-0044).

Therefore, Kim anticipates claim 12.

6.3 Regarding claims 13-15, the method and system of Kim is used as part of an In-Circuit Emulation system with the FPGA acting as a microcontroller. See page 2 paragraphs 0036-0044.

6.4 Regarding claims 16-26, these claims are anticipated using the reasoning above for claims 12-15, with synchronization and lock step operation provided through software programming of the FPGA 4 of clock frequency and single-step or multi-step stimulus. See page 3 paragraphs 0062-0068.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure. Reference to Voth, U. S. Patent 6,058,263 is cited as teaching an interface design using FPGAs that serve as programmable glue logic to connect discrete components of a computer system.

Reference to Thakkar, U. S. Patent Application Publication US 2002/0156885 A1 published 24 October 2002 and filed 23 April 2001, is cited as teaching a network protocol emulator.

Reference to Bursky, "FPGA Combines Multiple Interfaces and Logic," Electronic Design, Vol. 48 No. 20, pp. 74-78 (2 October 2000), is cited as teaching PCI, Utopia, 10/100, Ethernet, etc. interfaces implemented by FPGAs.

Reference to Anonymous, "Warp Nine Engineering – The IEEE 1284 Experts – F/Port Product Sheet," undated web page found at http://www.fapo.com/fport.htm, describes the downloading of F/Port hardware "personalit[ies]" used to make a parallel port look like a printer.

Reference to Anonymous, "F/Port: Fast Parallel Port for the PC: Installation Manual: Release 7.1," circa 1997, available for download from http://www.fapo.com/fport.htm, describes the downloading of F/Port hardware "personalities" used to make a parallel port look like a printer.

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (571) 272-3709. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (571) 272-2100.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER